

Verilog Coding for Logic Synthesis

By Weng Fook Lee

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Provides a practical approach to Verilog design and problem solving.
* Bulk of the book deals with practical design problems that design engineers solve on a daily basis.
* Includes over 90 design examples.
* There are 3 full scale design examples that include specification, architectural definition, micro-architectural definition, RTL coding, testbench coding and verification.
* Book is suitable for use as a textbook in EE departments that have VLSI courses

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Editorial Review

From the Back Cover
A practical introduction to writing synthesizable Verilog code

Rapid change in IC chip complexity and the pressure to design more complex IC chips at a faster pace has forced design engineers to find a more efficient and productive method to create schematics with large amounts of logic gates. This has led to the development of Verilog; one of the two types of Hardware Description Language (HDL) currently used in the industry.

Verilog Coding for Logic Synthesis is a practical text that has been written specifically for students and engineers who are interested in learning how to write synthesizable Verilog code. Starting with simple verilog coding and progressing to complex real-life design examples, Verilog Coding for Logic Synthesis prepares you for a variety of situations that are bound to occur while utilizing Verilog.

Expert design engineer Weng Fook Lee:

- Introduces the usage of Verilog and VHDL
- Describes a design flow for ASIC design
- Discusses basic concepts of Verilog coding
- Explores the common practices and coding style that are used when coding for synthesis and shows you the common coding style on Verilog operators
- Explains how a design project of a programmable timer is implemented
- Reveals the design of a programmable logic block for peripheral interface

Filled with practical advice, functional flowcharts and waveforms, and over ninety examples, Verilog Coding for Logic Synthesis will help you fully understand the concepts and coding style of important industry language.

About the Author
WENG FOOK LEE is a prominent member of the Technical Staff (MTS) at Advanced Micro Devices (AMD) Design Center. He has vast experience in designing with Verilog and VHDL, and is an acknowledged expert in the field of RTL coding and logic synthesis. Lee is an expert at synthesizing and tweaking design synthesis, and in developing and implementing new logic verification, synthesis, auto-place-route, and back-annotation design methodology. He has experience in the design and synthesis of PCI, ISA and LPC bridges, chipsets, microcontrollers, RISC microprocessors, and state-of-the-art, high-speed, low-power flash memory.

Users Review

From reader reviews:

Greg Wilson:

As people who live in the actual modest era should be change about what going on or facts even knowledge to make these keep up with the era that is certainly always change and advance. Some of you maybe will update themselves by studying books. It is a good choice to suit your needs but the problems coming to you actually is you don't know what kind you should start with. This Verilog Coding for Logic Synthesis is our

recommendation to cause you to keep up with the world. Why, because book serves what you want and need in this era.

Linda Porter:

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